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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,910	04/21/2004	Vincent Nguyen	200316223-1	5643

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EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,910	NGUYEN ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6 and 11-20* is/are rejected.

7)☒ Claim(s) *4 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Paragraph 14, line 3 refers to the keyboard as item 24 in Figure 1, when it appears it should be labeled item 26.

Appropriate correction is required.

Claim Objections

Claim 3 recites the limitation "the bus" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is ambiguous what applicant means by "selecting the first and second slots to correspond to the width of the bus."

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. It is ambiguous what applicant means by "sizing the first and second slots larger than the size of first and second portions."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harwer et al. in view of Chan et al., and further in view of Zatorski.

With regard to claim 1, Harwer et al. teach a computer system, comprising:

A central processing unit (CPU) (Figure 1, item 10);

A first slot configured to receive a device (Figure 1, item 28; column 4, line 4; where a slot may be interpreted as an ISA bus connector);

A second slot configured to receive a device (Figure 1, item 30; column 4, lines 12 – 14; where a slot may be interpreted as a processor direct connector);

At least one trace coupled to the first and second slots (Harwer et al. inherently teach this limitation since both slots are taught on a motherboard (Figure 1, item 1). Without at least one trace connecting to either slot, the slots would offer no functionality);

Whereby the computer system is configured so that inserting a jumper board in the first slot couples the first portion of the bridge to the second slot (where a jumper board may be interpreted as a combination ISA bus riser card/local bus translator card; Figure 1, item 40);

Harwer et al. fail to teach a bridge. However, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include a bridge connected to the CPU as well as the first and second slots for the purpose of allowing communication between the CPU and the slots. Chan et al. evidence this in column 4, lines 21 – 31 and also Zatorski in paragraphs 4 – 6. Additionally, it would have been obvious to connect a first portion of the bridge to the first slot, and a second portion of the bridge to the second slot for similar rationale.

With regard to claim 2, Zatorski teaches that bridges are used to couple one bus to another, as well as connect a processor bus to a peripheral bus. Therefore, Zatorski inherently teaches that the first and second portions of the bridge comprise a bus, since a bridge functions only to link buses to one another (paragraphs 4 – 6).

With regard to claim 3, Harwer et al. implicitly teach the limitation wherein each slot is capable of providing all signals pertaining to the bus by definition of each slot. Harwer et al. teach the first slot as an ISA bus connector, therefore, by definition, the slot includes all signals pertaining to the ISA bus. Harwer et al. teach the second slot as a processor direct connector, which provides all signals pertaining to a local bus (column 4, lines 12 – 18).

* * *

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harwer et al. in view of Chan et al., in view of Zatorski, and further in view of Intel Corporation.

With regard to claims 5 and 6, Harwer et al., Chan et al., and Zatorski al fail to teach lane polarity inversion and lane reversal implemented on a printed circuit board that includes the first and second slots.

Intel Corporation teach using lane polarity inversion and lane reversal for the purposes of eliminating "bowties" on a printed circuit board (page 7, section 1.2.2 – page 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate lane polarity inversion and lane reversal techniques on a printed circuit board that includes the first and second slots for the

purpose of reducing and/or eliminating "bowties." This would have been obvious in order to reduce the cost of the PCB by reducing the size, complexity, or number of necessary layers.

* * *

Claims 11, 12, 15, and 16 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harwer et al.

With regard to claim 11, Harwer et al. teach a method of providing a bus in a computer system comprising:

Routing a first portion of the bus to a first segment of a first slot (where a first slot may be interpreted as a processor-direct connector; Figure 1, item 30; column 4, lines 12 – 18); Examiner interprets the first portion of the bus as the superset of local bus signals are described in column 4, lines 12 - 18);

Routing a second portion of the bus to a first segment of a second slot (where a second slot may be interpreted as an ISA bus connector; Figure 1, item 28; Examiner interprets a second portion of the bus as the portion containing signals necessary for operation of the ISA bus connector);

Coupling a second segment of the first slot to a second segment of the second slot (Examiner identifies riser card (Figure 1, item 40) as coupling a second segment of the first and second slots);

Inserting a jumper board (Figure 1, item 40) into the first slot (Figure 1, item 30);

Wherein the jumper board connects the first and second segments of the first slot, thereby routing the first portion of the bus to the second slot (Examiner interprets the connector (Figure 1, item 42) as connecting the first and second segments of the first slot).

With regard to claim 12, Harwer et al. teach the additional limitation wherein the first and second portions of the bus comprise the entire bus since Examiner interprets the first portion as a superset of all local bus signals, and the second portion as only ISA bus signals; the union of both sets would comprise the entire set of signals, or the entire bus.

With regard to claim 15, Harwer et al. teach the additional limitation wherein the first and second slots are capable of providing all signals that pertain to the entire bus (column 4, lines 12 – 18 indicate that the first slot, interpreted as a processor-direct connector is able to provide a superset of signals which enable any local bus to be implemented. Examiner interprets the second slot as providing only ISA bus signals, however, the union of both sets of signals for both slots (or even, just the first slot alone) would provide signals for the entire bus, and therefore meets this limitation).

With regard to claim 16, Harwer et al. teach the additional limitation wherein the connection between slots occurs on a system board (where Figure 1, item 40 may be interpreted as a system board, which connects both slots (Figure 1, items 28, 30));

With regard to claim 17, Harwer et al. teach a computer system, comprising:

Means for allocating a bus among a first and a second slot (where a first slot may be interpreted as an ISA bus connector; Figure 1, item 28; where a second slot may be interpreted as a processor-direct connect; Figure 1, item 30; column 4, lines 12 – 18);

Means for coupling at least two portions of a first slot together ((Examiner interprets the connector (Figure 1, item 44) as connecting the first and second segments of the first slot).

Whereby the second slot is capable of providing the entire bus (column 4, lines 12 – 18);

With regard to claim 18, Harwer et al. teach the additional limitation wherein the means for coupling a portion of the first slot to a portion of the second slot comprises traces on a system board (where Figure 1, item 40 may be interpreted as a system board, which connects both slots (Figure 1, items 28, 30));

With regard to claim 19, Harwer et al. teach the additional limitation wherein the means for coupling at least two portions of the first slot together comprises a jumper board (where Figure 1, item 40 may be interpreted as a jumper board).

* * *

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harwer et al. in view of Intel Corporation.

With regard to claim 20, Harwer et al., Chan et al., and Zatorski al fail to teach a means for reducing the number of bowtie connections in a system.

Intel Corporation teach using lane polarity inversion and lane reversal for the purposes of reducing/eliminating "bowties" on a printed circuit board (page 7, section 1.2.2 – page 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate lane polarity inversion and lane reversal techniques in the system of Harwer et al. for the purpose of reducing and/or eliminating "bowties." This would have been obvious in order to reduce the cost of the PCB by reducing the size, complexity, or number of necessary layers.

Allowable Subject Matter

Claims 4, and 7 - 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
2/15/06